

IN THE CLAIMS:

Prior to examination, please cancel claims 1-28, and add the following new claims 29-57.

29. (New) A processor comprising:
at least one critical memory structure to detect an error; and
a processor error processing logic hardware coupled to the at least one critical memory structure. The processor error processing logic hardware to store a physical address of an errant process that caused the error, store an execution instruction pointer (IP) in an interruption instruction pointer (IIP), determine a first virtual address from an operating system mapping table, determine a second virtual address from a translation look-aside buffer, and identify the errant process, if the physical address and the second virtual address match the physical address and the first virtual address.
30. (New) The processor of claim 29 wherein the processor error processing logic hardware is further to:
determine whether the physical address of the physical memory location is known;
determine in which code section the errant process is located, if the physical memory location is known;
reset the processor, if the physical memory location is in one of a critical section and an unknown section of the code; and
terminate the errant process based on a level of sharing of the physical memory location and whether the IIP associated with the errant process is precise, if the physical memory location is in a non-critical section of the code.
31. (New) The processor of claim 29 wherein the processor error processing logic hardware is to store the physical address of the errant process that caused the error in a memory register.

32. (New) The processor of claim 29 wherein the processor error processing logic hardware to determine the first virtual address from the operating system mapping table comprises:

the processor error processing logic hardware to find a physical address entry in the operating system mapping table that matches the physical address, and to read the first virtual address from the matching physical address entry, if the matching physical address entry is found.

33. (New) The processor of claim 29 wherein the processor error processing logic hardware to determine the second virtual address from the translation look-aside buffer comprises:

the processor error processing logic hardware to find a physical address entry in the translation look-aside buffer that matches the physical address, and to read the second virtual address from the matching physical address entry, if the matching physical address entry is found.

34. (New) The processor of claim 29 wherein said execution instruction pointer comprises:

an instruction pointer that existed at the time the error is detected.

35. (New) The processor of claim 29 wherein the processor error processing logic hardware comprises:

a register to store the physical address of the errant process.

36. (New) The processor of claim 29 wherein the processor error processing logic hardware comprises:

an interruption instruction pointer register to store the execution instruction.

37. (New) The processor of claim 29 wherein said at least one critical memory structure comprises at least one of:

an error correcting code protected memory structure; and
a parity protected memory structure.

38. (New) The processor of claim 37 wherein said error correcting code protected memory structure to assert an error signal, if said error correcting code protected memory structure detects an error.

39. (New) The processor of claim 37 wherein said error correcting code protected memory structure to assert the error signal to the processor error processing logic hardware.

40. (New) The processor of claim 37 wherein said parity protected memory structure to assert an error signal, if said parity protected memory structure detects an error.

41. (New) The processor of claim 40 wherein said parity protected memory structure to assert the error signal to the processor error processing logic hardware.

42. (New) A computer system, comprising:
a system memory; and
a processor coupled to the system memory, the processor comprising:
at least one critical memory structure to detect an error; and
a processor error processing logic hardware coupled to the at least one critical memory structure, the processor error processing logic hardware to store a physical address of an errant process that caused the error, store an execution instruction pointer (IP) in an interruption instruction pointer (IIP), determine a first virtual address from an operating system mapping table, determine a second virtual address from a translation look-aside buffer, and identify the errant process, if the physical address and the second virtual address match the physical address and the first virtual address.

43. (New) The computer system of claim 42 wherein said processor error processing logic hardware comprises:

an errant process physical address register to store the physical address of the errant process that caused the error.

44. (New) The computer system of claim 42 wherein said processor error processing logic hardware comprises:

an IIP register to store the execution IP.

45. (New) The computer system of claim 42 further comprising:
a mapping table to maintain a mapping between all virtual addresses and all physical addresses in the computer system so that each virtual address is mapped to one physical address.

46. (New) The computer system of claim 45, wherein the mapping table is implemented as:

a buffer.

47. (New) The computer system of claim 45, wherein the mapping table is implemented as:

a cache array.

48. (New) A computer system, comprising:

a system memory; and

a plurality of processors coupled to the system memory, each of the plurality of processors comprising:

at least one critical memory structure to detect an error; and

a processor error processing logic hardware coupled to the at least one critical memory structure, the processor error processing logic hardware to detect an error, store a physical address of an errant process that caused the error, store an execution instruction pointer (IP) in an interruption instruction pointer (IIP), determine a first virtual address from an operating system mapping table, determine a second virtual address from a translation look-aside buffer and identify the errant process, if the physical address and the second virtual address match the physical address and the first virtual address.

49. (New) The computer system of claim 48 wherein said memory register comprises:

an errant process physical address to receive and store the physical address of the errant process that caused the error.

50. (New) The computer system of claim 48 further comprising:
a mapping table to maintain a mapping between all virtual addresses and all physical addresses in the computer system so that each virtual address is mapped to one physical address.

51. (New) The computer system of claim 50 wherein the mapping table is implemented as:
a buffer.

52. (New) The computer system of claim 50 wherein the mapping table is implemented as:
a cache array.

53. (New) The computer system of claim 50 wherein each of the plurality of processors further comprises:
a translation look-aside buffer (TLB) to store physical addresses.

54. (New) The computer system of claim 53 wherein the TLB is further to store second virtual addresses associated with the physical addresses.

55. (New) The computer system of claim 53 further comprising:
a firmware component to provide the physical addresses stored in the TLB.

56. (New) The computer system of claim 55 wherein said firmware component further to provide the second virtual addresses stored in the TLB.

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57. (New) The computer system of claim 48 wherein said at least one critical memory structure comprises at least one of:
an error correcting code protected memory structure; and
a parity protected memory structure.